ABSTRACT OF THE DISCLOSURE

The present invention provides a data processing apparatus and method for performing a data processing operation on first and second floating point data elements, the first floating point data element specifying a first exponent and the second floating point data element specifying a second exponent. The data processing apparatus comprises processing logic providing multiple processing paths which are selectable to perform the data processing operation, including a first processing path operable to perform the data processing operation if a predetermined alignment condition exists. Further, at least one detector logic unit is provided which is operable to receive both the first exponent and the second exponent and to detect the presence of the predetermined alignment condition. Each detector logic unit comprises half adder logic operable to perform a half adder operation to logically subtract one of the first and second exponents from the other of the first and second exponents to produce at least a sum data value of sum and carry data values representing the result of the half adder operation. Further, each detector logic unit comprises generation logic operable to receive the sum data value and to generate a select signal which is set if the sum data value has a predetermined value indicating the existence of the predetermined alignment condition. The processing logic is then operable to select the first data processing path to perform the data processing operation if the select signal from one of the at least one detector logic units is set. The particular structure of detector logic unit provided enables a fast detection of the existence of the predetermined alignment condition, which enables an early selection of the first data processing path if the select signal is set. This enables significant power and area savings to be made.